**Ibrahim Rupawala**

**San Jose, CA Linkedin:** [**https://www.linkedin.com/in/irupawala/**](https://www.linkedin.com/in/irupawala/)

**Mobile: +1(480) 284 – 9270 Github:** [**https://github.com/irupawala**](https://github.com/irupawala)

**Email:** [**ibrahimrupawala@gmail.com**](mailto:ibrahimrupawala@gmail.com)

***EDUCATION***

**Master of Science, Electrical and Computer Engineering Dec 2017**

Arizona State University, Tempe, USA

**Bachelor of Engineering, Electronics Engineering May 2013**

Gujarat Technological University, Gujarat, India

***TECHNICAL SKILLS***

**Programming Languages:** Python, C++

**Database Technologies:** Postgre SQL, MongoDB

**Frameworks & Packages:** Node JS, Pandas, Numpy, Matplotlib, Scikit

**Tools & Technologies:** Visual Studio Code, Express, Matlab, React, JIRA, Git, Jupyter Notebook, Matlab

**Related Coursework:** Data Structures and Algorithms, System Design, Computer Architecture, OOP Design, Operating Systems

***WORK EXPERIENCE***

**Staff Software Engineer, Western Digital Technologies, Milpitas, CA Jan 2018 - Present**

* Development and Optimization of Error Correction Code Algorithms for enterprise level solid-state drives.
* Integration and validation of media system algorithms and architecture for next generation products.
* Performance Modelling of the solid-state drives to evaluate performance and analyze trade-offs.
* Develop and automate reliability test data collection, parsing, cleaning and visualization with Python.
* Optimize performance, endurance, reliability of solid-state drive (SSD) products for the target markets

**Software Engineering Intern, Micron Technologies, Milpitas, CA May 2017 - Dec 2017**

* Define and develop system and memory diagnostic software tools.
* Write software to verify and reproduce system wide software failure modes.
* Design and implement automation for System Level testing.
* Design, develop, test, and release software related to the Factory Automation software architecture.

**Graduate Teaching Assistant, Arizona State University, Tempe, AZ Oct 2016 - May 2017**

* Helped students in performing lab assignments using cadence environment for the course Analog & Digital Circuits.

**IC Design Intern, Analog Rails, Tempe, AZ May 2016 - Jul 2017**

* Designed standard cell library and performed characterization of the cells. Performed RTL verification of the cells.
* Characterized standard cell library creating models for delay, function, constraints, and power that efficiently model cell behavior. Developed the Layout of standard cells in 45 nm PDK and performed DRC and LVS checks.

***PROJECTS***

* **Phi X174 Genome Sequence Assembler**

Developed an assembler to recreate Genome Sequence from 100 nucleotides long 5386 error prone reads using Hamiltonian and Eulerian Path in Overlap Graph and DeBruijn Graph respectively. Removed tips and handled bubbles in the sequence.

* **Advanced Shortest Paths Algorithms**

Implemented Contraction Hierarchies Algorithm that results in 1000 times faster query performance compared to Dijkstra's algorithm on graphs for road networks. Also Implemented Bidirectional Djikstra, A-Star Algorithm

* **SODUKO Helper using Minisat SAT Solver**

Developed a SUDOKU Helper by feeding set of clauses in CNF Form to Minisat Solver to find the satisfying assignment.

* **Twitter Sentiments Analysis**

Trained the Naive Bayes classifier Model to predict sentiment from thousands of Twitter tweets. Performed tokenization to tweet text using Scikit Learn. Performed text data cleaning and removed punctuation and stop words.

* **Facial Expression Recognition using Keras**

Build and trained a convolutional neural network (CNN) in Keras from scratch to recognize facial expressions. The objective is to classify each face into one of seven categories (Angry, Disgust, Fear, Happy, Sad, Surprise, Neutral).

* **Restaurant NLU Chatbot with Rasa and Python**

Developed a Chatbot using ZOMATO API which can answer customer questions and can search restaurant, make reservations, validate cuisine, etc. Trained the NLU Model and validated the responses.

* **MIPS R3000 5 Stage pipelined microprocessor with Data Forwarding & Branch Delay Slot**

Designed and verified MIPS R3000 core with Data Hazard Detection, Data Forwarding, Control Hazard Detection & Branch Delay Slot in System Verilog with an IPC of 0.90.

* **Design of hardware accelerator for single source shortest path (SSSP) Dijkstra Algorithm**

Designed a hardware accelerator for Dijkstra’s Algorithm. Mapped the design into Xilinx Virtex 7 XC7VX485T‐ 2FFG1761 FPGA and 28nm ASIC target and extracted area, power and timing reports.

***ACHIEVEMENTS***

* Gold Medal for Consistent Academic Performance by Gujarat Technological University, India
* Merit based award for Outstanding Academic Performance by Ministry of HR Development, India
* Outstanding Teaching Assistant Award and Tuition fees waiver by Arizona State University, USA
* MVP and Platinum performance Awards by Western Digital Technologies